IN THE CLAIMS

1. (Withdrawn) A method of fabricating a semiconductor device, comprising:

forming an initial high voltage gate insulation layer on a low voltage region of a semiconductor substrate;

forming a pad insulation layer on a high voltage region of the semiconductor substrate, the pad insulation layer being formed to be thinner than the initial high voltage gate insulation layer;

forming a plurality of mask patterns on the pad insulation layer and the initial high voltage gate insulation layer;

etching the pad insulation layer, the initial high voltage gate insulation layer and the semiconductor substrate using the hard mask patterns as etching masks to form first and second trench regions in the low voltage region and the high voltage region respectively, the first and second trench regions defining first active regions and second active regions respectively;

forming first and second isolation layers in the first and second trench regions respectively;

removing the hard mask patterns and the pad insulation layer to expose the first active regions and the initial high voltage gate insulation layer; and

forming a low voltage gate insulation layer on the exposed first active regions, the low voltage gate insulation layer being formed to be thinner than the initial high voltage gate insulation layer.

2. (Withdrawn) The method of claim 1, wherein the low voltage region corresponds to a low voltage MOS transistor region, and the high voltage region corresponds to a high voltage MOS transistor region.

3. (Withdrawn) The method of claim 1, wherein the low voltage region corresponds to a cell array region, and the high voltage region corresponds to a high voltage MOS transistor region of a peripheral circuit region.

4. (Withdrawn) The method of claim 1, wherein forming the initial high voltage gate insulation layer and the pad insulation layer comprises:

forming an initial high voltage gate oxide layer on an entire surface of the semiconductor substrate;

selectively removing the initial high voltage gate oxide layer in the low voltage region to expose the semiconductor substrate in the low voltage region; and

thermally oxidizing the substrate where the initial high voltage gate oxide layer in the low voltage region is removed to form a pad oxide layer on the exposed semiconductor substrate, the pad oxide layer being formed to be thinner than the initial high voltage gate oxide layer.

5. (Withdrawn) The method of claim 4, wherein forming an initial high voltage gate oxide layer comprises thermal oxidation.

6. (Withdrawn) The method of claim 1, wherein forming the hard mask patterns comprises:

forming a hard mask layer on an entire surface of the substrate having the initial high voltage gate insulation layer and the pad insulation layer; and

patterning the hard mask layer.

7. (Withdrawn) The method of claim 6, wherein forming a hard mask layer comprises sequentially stacking a lower hard mask layer and an upper hard mask layer.

8. (Withdrawn) The method of claim 7, wherein the lower hard mask layer is formed of a first material layer having an etch selectivity with respect to the initial high voltage gate insulation layer, the pad insulation layer and the semiconductor substrate, and the upper hard mask layer is formed of a second material layer having an etch selectivity with respect to the semiconductor substrate.

9. (Withdrawn) The method of claim 8, wherein the first material layer is formed of a silicon nitride layer, and the second material layer is formed of a silicon oxide layer.

10. (Withdrawn) The method of claim 6, wherein the hard mask layer is formed of a single layer of material having an etch selectivity with respect to the initial high voltage gate insulation layer, the pad insulation layer and the semiconductor substrate.

11. (Withdrawn) The method of claim 10, wherein the single layer of material is a silicon nitride layer.

12. (Withdrawn) The method of claim 1, wherein forming the first and second isolation layers comprises:

forming an insulation layer filling the trench regions on an entire surface of the substrate having the first and second trench regions; and

planarizing the insulation layer until the hard mask patterns are lo exposed.

13. (Withdrawn) The method of claim 1 further comprises forming a thermal oxide layer at inner walls of the first and second trench regions prior to formation of the first and second isolation layers.

14. (Withdrawn) The method of claim 1, wherein the low voltage gate insulation layer is a thermal oxide layer.

15. (Withdrawn) The method of claim 1, further comprising:

forming a first conductive layer on an entire surface of the substrate having the low voltage gate insulation layer; and

patterning the first conductive layer to form low voltage gate electrodes crossing over the first active regions and high voltage gate electrodes crossing over the second active regions.

16. (Withdrawn) The method of claim 1, further comprising:

forming a first conductive layer on an entire surface of the substrate having the low voltage gate insulation layer;

patterning the first conductive layer to form floating gate patterns covering the first active regions and a main gate pattern covering the high voltage region;

sequentially forming an inter-gate dielectric layer and a second conductive layer on an entire surface of the substrate having the floating gate patterns and the main gate pattern; and

patterning the second conductive layer, the inter-gate dielectric layer, the floating gate patterns and the main gate pattern to form control gate electrodes crossing over the first active regions as well as floating gates interposed between the control gate electrodes and the low voltage gate insulation layer, and to simultaneously form a main gate electrode and a

dummy gate electrode, which are sequentially stacked over the second active region and are formed to cross over the second active region.

17. (Withdrawn) The method of claim 1 further comprising forming spacers on sidewalls of the hard mask patterns prior to formation of the first and second trench regions, wherein the first and second trench regions are formed by etching the semiconductor substrate using the hard mask patterns and the spacers as etching masks, and the spacers are removed prior to formation of the first and second isolation layers.

18. (Withdrawn) A method of fabricating a semiconductor device, comprising:

forming an initial high voltage gate oxide layer on an entire surface of a semiconductor substrate having a low voltage MOS transistor region and having a high voltage MOS transistor region;

patterning the initial high voltage gate oxide layer to selectively expose the semiconductor substrate in the low voltage MOS transistor region;

forming a pad oxide layer on the exposed semiconductor substrate in the low voltage MOS transistor region to a thickness thinner than the initial high voltage gate oxide layer;

forming a plurality of hard mask patterns on the substrate having the pad oxide layer;

forming spacers on sidewalls of the hard mask patterns;

etching the pad oxide layer, the initial high voltage gate oxide layer and the semiconductor substrate using the hard mask patterns and the spacers as etching masks to form first trench regions defining first active regions in the low voltage MOS transistor region and second trench regions defining second active regions in the high voltage MOS transistor region;

removing the spacers;

forming an insulation layer to fill the first and second trench regions on an entire surface of the substrate where the spacers are removed;

planarizing the insulation layer until the hard mask patterns are exposed to form first and second isolation layers in the first and second trench regions respectively;

removing the hard mask patterns and pad oxide layer to expose the first active regions and the initial high voltage gate oxide layer; and

forming a low voltage gate oxide layer on the exposed first active regions to a thickness thinner than the initial high voltage gate oxide layer.

19. (Withdrawn) The method of claim 18, wherein forming spacers comprises forming a silicon oxide layer or a silicon nitride layer.

20. (Withdrawn) The method of claim 18, further comprising:

etching the pad oxide layer, the initial high voltage gate oxide layer and the semiconductor substrate using the hard mask patterns as etching masks prior to formation of the spacers to form first recessed regions that define first active regions in the low voltage MOS transistor region and second recessed regions that define second active regions in the high voltage MOS transistor region, the spacers being formed to cover sidewalls of the hard mask patterns and sidewalls of the first and second recessed regions and the first and second trench regions being formed by etching the semiconductor substrate using the hard mask patterns and the spacers as etching masks; and

thermally oxidizing the semiconductor substrate where the spacers are removed, prior to formation of the insulation layer filling the first and second trench regions to form a thermal oxide layer at inner sidewalls of the first and second recessed regions and the first and second trench regions.

21. (Withdrawn) The method of claim 18, wherein forming spacers comprises forming a thermal oxide layer, a chemical vapor deposition (CVD) oxide layer or a chemical vapor deposition (CVD) nitride layer.

22. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate having a low voltage region and a high voltage region;

a first isolation layer formed in the low voltage region and defining a first active region;

a second isolation layer formed in the high voltage region and defining a second active region;

a low voltage gate insulation layer formed on the first active region; and

a high voltage gate insulation layer formed on the second active region and having a greater thickness than the low voltage gate insulation layer, wherein a top surface of the second isolation layer is higher than that of the high voltage gate insulation layer, a step region between the high voltage gate insulation layer and the second isolation layer has no recessed region ~~a profile with no portion without any recessed region that is lower than the top surface of the high voltage gate insulation layer~~, and wherein the step region is spaced

apart from a vertical axis passing through an edge corner of the second active region toward the second isolation layer adjacent to the vertical axis.

23. (Original) The semiconductor device of claim 22, further comprising:

a low voltage gate electrode formed on the low voltage gate insulation layer, the low voltage gate electrode crossing over the first active region; and

a high voltage gate electrode formed on the high voltage gate insulation layer, the high voltage gate electrode crossing over the second active region.

24. (Original) The semiconductor device of claim 22, wherein the low voltage region is a memory cell array region.

25. (Original) The semiconductor device of claim 24, wherein the low voltage gate insulation layer is a tunnel oxide layer.

26. (Currently amended) The semiconductor device of claim 22, further comprising:

a control gate electrode formed over the low voltage gate insulation layer, the control gate electrode crossing over the first active region;

a floating gate interposed between the control gate electrode and the low voltage gate insulation layer;

a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode crossing over the second active region;

a dummy gate electrode stacked on the main gate electrode; and

an inter-gate dielectric layer interposed between the floating gate and the control gate.

27. (Original) The semiconductor device of claim 22 further comprising a thermal oxide layer interposed between the first isolation layer and the semiconductor substrate, and between the second isolation layer and the semiconductor substrate.

28. (Original) The semiconductor device of claim 22, wherein an edge region of the first isolation layer is lower than a top surface of the low voltage gate insulation layer.

29. (Currently amended) A semiconductor device comprising:

a semiconductor substrate having a low voltage region and a high voltage region;

a first trench region formed in the low voltage region to define a first active region, the first active region having a protruded edge surface;

a first sloped region interposed between the first trench region and the first active region, the first sloped region having a first incline that is downwardly extended from the protruded edge surface of the first active region;

a second trench region formed in the high voltage region to define a second active region, the second active region having a relatively flat top surface;

a second sloped region interposed between the second active region and the second trench region, the second sloped region having a second incline that is downwardly extended from the edge corner of the ~~first~~ second active region;

a first isolation layer filling the first trench region and covering the first incline;

a second isolation layer filling the second trench region and covering the second incline;

a low voltage gate insulation layer formed on the first active region, the low voltage gate insulation layer having a top surface lower than a top surface of the first isolation layer; and

a high voltage gate insulation layer formed on the second active region, the high voltage gate insulation layer having a flat top surface lower than a top surface of the second isolation layer and being thicker than the low voltage gate insulation layer, the top surfaces of the low voltage gate insulation layer and the high voltage gate insulation layer having a profile without any recessed regions.

30. (Original) The semiconductor device of claim 29, wherein the low voltage gate insulation layer on the protruded edge surface of the first active region is thinner than the low voltage gate insulation layer on ~~the~~ a central region of the first active region

31. (Original) The semiconductor device of claim 29, wherein a vertical axis passing through the edge of the top surface of the low voltage gate insulation layer is located in the first sloped region.

32. (Currently amended) The semiconductor device of claim 33~~claim 29~~, wherein a distance between an ~~the~~ upper corner of the first trench region and a lower corner of the low

voltage gate electrode ~~and the low voltage gate insulation layer~~ is greater than the thickness of the low voltage gate insulation layer.

33. (Original) The semiconductor device of claim 29, further comprising:

a low voltage gate electrode formed on the low voltage gate insulation layer and disposed to cross over the first active region; and

a high voltage gate electrode formed on the high voltage gate insulation layer and disposed to cross over the second active region.

34. (Original) The semiconductor device of claim 29, wherein the low voltage region is a memory cell region.

35. (Original) The semiconductor device of claim 34, wherein the low voltage gate insulation layer is a tunnel oxide layer.

36. (Original) The semiconductor device of claim 35, further comprising:

a control gate electrode formed over the tunnel oxide layer and disposed to cross over the first active region;

a floating gate interposed between the control gate electrode and the tunnel oxide layer;

an inter-gate dielectric layer interposed between the floating gate and the control gate electrode;

a main gate electrode formed on the high voltage gate insulation layer and disposed to cross over the second active region; and

a dummy gate electrode stacked on the main gate electrode.